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Our Ref. No.: 082225.P0189R

413-ESD

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application for:

M. Powell et al.

Serial No.: 08/887,680

Filed: July 3, 1997

For: **METHOD AND APPARATUS FOR EXTENDING COMPUTER ARCHITECTURE FROM 32 TO 64 BITS**

AMENDMENT

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

Please amend the above-identified application as follows:

IN THE CLAIMS

33. (Amended) A method for context switching a processor that executes procedures having differing word sizes, comprising the steps of:

testing a least significant bit of a stack pointer register in the processor that indicates whether a set of data values for a procedure that are stored in a set of registers in the processor, each have a first word size or a second word size, wherein the first word size is less than the second word size;

transferring the data values from a least significant portion of each register to a first stack save area in memory if the least significant bit of the stack pointer register indicates the first word size;

transferring the data values from the registers to a second stack save area in memory if the least significant bit of the stack pointer register indicates the second word size[;

setting a width indication bit in the first stack save area in memory, and transferring the data values from the registers to a second stack save area in memory and transferring the stack pointer value